In the specification:

In the Brief Description of the Drawings section, please add the following paragraph after paragraph **[0017]**:

FIG. 5 is a flowchart illustrating a method for writing back cache lines in accordance with embodiments of the invention.

Please replace paragraph **[0042]** with the following amended paragraph:

[0042] For example, if the core processor (as opposed to a general processor that typically includes the core processor and memory) receives an instruction to write data to memory location 206, and memory location 206 indexes to cache lines in associated set 230, then **[[**the**]]** a cache controller could write to any two available cache lines in the associated set 230. Thus, if cache lines 214 and 216 are available, then the controller would write to those two cache lines. Furthermore, if no cache lines are available, the cache controller would invoke a replacement policy (to be discussed) to free up cache lines.

Please replace paragraph **[0047]** with the following amended paragraph:

[0047] Cache line is not corrupt: If the line is not corrupt, then the cache line is written back to a corresponding memory location at block 416 [[414]], as determined by the tag address of the cache line. At block 418, the cache line is marked available.

Please replace paragraph **[0053]** with the following amended paragraph:

[0053] If the current memory location has been written to, then associated cache lines are found and marked invalid. (However, as illustrated in FIG. 5, even once a memory location has been

written back to, corresponding cache lines may still be read to achieve a high confidence level that the data being written back is valid. Using this approach, the lines may be marked accordingly - i.e., if a line is not corrupt, it can be marked available - clean or dirty - and if a line is corrupt, it is marked invalid. While either implementation is within the scope of the invention, described embodiments use the former of these two implementations.) When no more associated cache lines exist, the method ends at block 420.

Please replace paragraph **[0059]** with the following amended paragraph:

[0059] Furthermore, the mechanism is congruent with existing methods of data recovery. For example, in an implementation where both dirty cache lines are read to achieve a high confidence of valid data, if the second cache line is corrupt, it can be scrubbed using the uncorrupt data from the first cache line. As another example, if one of the cache lines becomes permanently non-functional, the capability to run the cache in degraded mode means that the part of the cache containing the non-functional cache line may be ignored with the advantage that the first cache line is not functional, and may ~~contains~~ contain good data.